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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,634	03/17/2000	Sun Man Lo	10262-013100US	3050

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EXAMINER	
SORRELL, ERON J	

ART UNIT	PAPER NUMBER
2182	13

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,634	LO ET AL.	
	Examiner	Art Unit	
	Eron J Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-10* is/are allowed.

6)☒ Claim(s) *1-6 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-6 and 11-13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim 1 and 13 recite the limitation, "... a delay circuit for delaying generation of the control signal for a programmable delay time related to ***transmission characteristics of said transmission line***." It is unclear to the Examiner what is included or not included by the phrase ***transmission characteristics of the transmission line*** (emphasis added).

DETAILED ACTION

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al. (U.S. Patent No. 5,287,458 hereinafter "Michael") in view of Applicant's admitted prior art (AAPA).

5. Referring to claim 1, Michael teaches a universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer (see item labeled 42 in figure 2);

a shift register coupled to the FIFO buffer (see item labeled 40 in figure 2);

a serial transmission line coupled to the shift register for connecting to a remote processor (see item 11 in figure 2 and 22-29 of column 4);

a circuit for detecting the last word transmitted from the FIFO buffer of the serial transmission line (see lines 7-30 of column 8);

a transmitter empty circuit for generating a control signal relating to the availability of the serial transmission line to receive data, on a control line when a last word transmitted from the FIFO buffer is detected (see lines 7-30 of column 8);

a delay circuit for delaying generation of the control signal for a programmable delay time (see lines 31-49 of column

15; Note that the delay is calculated using the time of the last stop bit. The number of stop bits is programmable (see lines 9-17 of column 5)); and

a programmable register for setting the programmable delay time (see lines 9-17 of column 5; Note the number of stop bits is programmable and is directly used in the delay time calculation).

Michael fails to teach the delay time is related to transmission characteristics of transmission lines.

The applicant admits at lines 26-33 of page 1 of the specification that it is common in the art to relate the delay time in a UART to transmission characteristics of the transmission line.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Michael with the AAPA. One of ordinary skill in the art would have been motivated to make such modification in order to customize the delay time if the user knows certain parameters concerning the transmission line.

6. Referring to claim 2, Michael teaches the control signal is triggered from the last stop bit of the last word (see lines 29-37 of column 1 and lines 7-30 of column 8).

7. Referring to claim 11, Michael teaches the stop bit is detected in the shift register (see lines 7-30 of column 8).

8. Referring to claim 12, Michael teaches the control signal is an RTS signal (see lines of 47-59 of column 1; Note the Examiner is relying on Applicant's definition of the RTS signal found at lines 12-17 of the applicant's specification).

9. Referring to claim 13, Michael teaches a universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer (see item labeled 42 in figure 2);

a shift register coupled to the FIFO buffer (see item labeled 40 in figure 2);

a serial transmission line coupled to the shift register for connecting to a remote processor (see item 11 in figure 2 and 22-29 of column 4);

a circuit for detecting the last word transmitted from the FIFO buffer of the serial transmission line (see lines 7-30 of column 8);

a transmitter empty circuit for generating a control signal relating to the availability of the serial transmission line to

receive data, on a control line when a last word transmitted from the shift register is detected (see lines 7-30 of column 8);

a delay circuit for delaying generation of the control signal for a programmable delay time (see lines 31-49 of column 15; Note that the delay is calculated using the time of the last stop bit. The number of stop bits is programmable (see lines 9-17 of column 5)); and

a programmable register for setting the programmable delay time (see lines 9-17 of column 5; Note the number of stop bits is programmable and is directly used in the delay time calculation).

Michael fails to teach the delay time is related to transmission characteristics of transmission lines.

The applicant admits at lines 26-33 of page 1 of the specification that it is common in the art to relate the delay time in a UART to transmission characteristics of the transmission line.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Michael with the AAPA. One of ordinary skill in the art would have been motivated to make such modification in

order to customize the delay time if the user knows certain parameters concerning the transmission line.

10. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael in view AAPA as applied to claims 1 and 13 above and further in view of Michael (U.S. Patent No. 5,140,679 hereinafter "Michael '679").

11. Referring to claim 5, the combination Michael and AAPA fails to teach the programmable register being a 4-bit register.

Michael '679 teaches the UART architecture can be of different sizes (see lines 28-47 of column 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Michael and AAPA with the teachings of Michael '679 such that the programmable register is a 4-bit register to reduce the amount of hardware in the system.

12. Referring to claim 6, the combination of Michael and AAPA teaches the delay circuit and the programmable register being a single circuit and the register connected to control the delay of the control signal for the channel (see lines 31-49 of column 15), however, Michael fails to teach there being a plurality of

channels, each channel having a FIFO buffer, the circuit for detecting the last word and the transmitter empty circuit.

Michael '679 teaches a UART comprising a plurality of channels, each channel having a FIFO buffer, the circuit for detecting the last word and the transmitter empty circuit (see lines 14-17 of column 1).

It would have been obvious to one of ordinary skill in the art at time of the applicant's invention to modify the combination of Michael and AAPA with the teachings of Michael '679 such that it comprises a plurality of channels each having a FIFO buffer, the circuit for detecting the last word and the transmitter empty circuit. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modification in order to allow the apparatus to transmit to a plurality of devices simultaneously.

Allowable Subject Matter

13. Claims 7-10 are allowed.

Response to Arguments

14. Applicant's arguments filed 2/17/04 have been fully considered but they are not persuasive. Applicant argues:

1) Michaels fails to teach the control signal in the transmitter empty circuit relates to the availability of the serial transmission line to receive data (see 3rd full paragraph of page 5 of applicant's remarks filed 2/17/04).

2) Michael excludes the extra Stop bit time, thus the variable number of stop bits is not used to produce the delay time (see 3rd full paragraph of page 5 of applicant's remarks filed 2/17/04).

As per argument 1, the Examiner disagrees. Michaels teaches the transmitter empty circuit is generated when the transmitter FIFO is empty. It is clear that when the transmission FIFO is empty it is in a condition to receive incoming data on the serial transmission line and it is requesting that such data be sent.

As per argument 2, the Examiner disagrees. Michaels teaches that the delay is directly calculated using the time of the ***last*** stop bit (emphasis added) at lines 31-49 of column 15. The number of stop bits is programmable and can be more than one (see lines 9-17 of column 5).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,619,458 to Benhamida teaches a UART with a programmable delay circuit.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
May 10, 2004

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100